REMARKS

Claims 1-29 and 31-32 are pending in the present application. The final rejection mailed on June 20, 2005, and the references cited therein have been considered. Favorable reconsideration is respectfully requested.

Claims 1, 2, 8, 28 and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Martel et al (U.S. patent no. 5,887,165). Claims 1, 2, 7, 19, 29 and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by O'Brien (U.S. patent no. 6,107,876). Claims 3 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Greif (WO 97/02570). Claims 4, 5, 9, 12, 13, 17, 18 and 25 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Wang (U.S. patent no. 5,765,027). Claims 10 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Todter et al (U.S. patent no. 5,937,070). Claim 16 was rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Keir (U.S. patent no. 5,467,400). Claims 20-22 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of McLaughlin et al. (U.S. patent no. 3,931,474). Claims 23 and 24 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Ledermann (U.S. patent

no. 6,278,784). Claim 27 was rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien/ Greif in view of Juszkiewicz et al (U.S. patent no. 6,353,169). Claim 26 was rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien/Greif in view of Suggs (U.S. patent no. 6,064,743). These rejections are respectfully traversed for the following reasons.

Claim 1 now recites a software definable pre-amplifier apparatus comprising one or a plurality of reconfigurable circuit means which are configured in real time under control of configuration data allowing said reconfigurable circuit means to implement, in hardware, different signal processing functions required for at least one of different digital signal processing algorithms and different audio processing protocols, a local memory coupled to said reconfigurable circuit means, the local memory storing the configuration data and being operative to supply configuration data to said reconfigurable circuit means when a different signal processing function is to be performed, and a host processor and associated program memory means for updating configuration data in said local memory and controlling and monitoring operation of the apparatus. Further, claim 1 has been amended to recite that the reconfigurable circuit means is reconfigured at a rate that

ensures that data input from at least one of a plurality of input channels and output from at least one of a plurality of output channels is processed in accordance with the required sampling rate or sampled data rate in a way that does not cause any signal aliasing and minimizes noise artifacts on any of the operative input and output channels in relation to the selected signal processing functions to be performed. This is not taught, disclosed or made obvious by the prior art of record.

Support for this amendment may be found in Applicants' specification as originally filed, for example, at paragraph [0014], [0028], [0032], [0059], and claim 11 as originally filed.

Applicants hereby incorporate by reference the remarks made in its previous responses in the parent application.

As noted previously, the only reconfigurable devices disclosed in the applied references are known as FPGA's which are incapable of being reconfigured in real time. Although the present Application does mention such devices, among a number of others, the claims of the present Application have been limited to devices that can be configured in real time, and thus to exclude devices of the FPGA type.

FPGA's are by definition field programmable and have to stop processing (be taken off line) and be reprogrammed with the relevant reconfiguration data. This can take many thousands of clock cycles. This is confirmed by the following information provided in a Xilinx datasheet, pages 1-16 of which were attached to Applicant's previous response. As described in the FPGA datasheets from Xilinx, an FPGA cannot operate while it is being configured. The I/O is tri-stated during the configuration stage and the device needs to go through an elaborate initialization routine before becoming functional again. Therefore, FPGA devices can't be configured in real time at a rate to implement different high-speed digital signal processing functions.

For many music applications the basic sampling rate is 44.1K samples per second (CD quality) or one sample every 0.0226 mSec. Consequently, it would not be possible to reconfigure an FPGA in real time to implement different digital signal processing algorithms or sub-functions. It takes too long to configure the device and many data samples would be lost.

Thus, FPGA's inherently have serious limitations that the present invention obviates by using reconfigurable circuit means that can be configured in real time, wherein the reconfigurable circuit means is reconfigured at a rate that

ensures that data input from at least one of a plurality of input channels and output from at least one of a plurality of output channels is processed in accordance with the required sampling rate or sampled data rate in a way that does not cause any signal aliasing and minimizes noise artifacts on any of the operative input and output channels in relation to the selected signal processing functions to be performed, as defined in claim 1 of the present application, to implement different functions. The apparatus according to the invention proves to be particularly advantageous in cases where audio processing algorithms are sequential in nature i.e. one sub-function or operation needs to be performed before the next. In the past, designers have designed an individual circuit for each sub-function or operation and then implemented all of the circuits on an ASIC device. However, by providing hardware circuitry that can be reconfigured in real time to implement the sub-functions as they are needed, the amount of circuitry is reduced. This then reduces the ASIC cost and overall system costs. It also allows the same programmable device to be reconfigured in real time to implement different audio processing standards, digital rights management schemes and post processing algorithms. Hence, this different type of programmable logic device obviates the limitations of FPGAs.

Martel discloses the configuration of the field programmable gate array at col. 4, line 64 to col. 5, line 19. However, neither this section, nor the rest of the patent discloses that the reconfigurable circuit means is reconfigured at a rate that ensures that data input from at least one of a plurality of input channels and output from at least one of a plurality of output channels is processed in accordance with the required sampling rate or sampled data rate in a way that does not cause any signal aliasing and minimizes noise artifacts on any of the operative input and output channels in relation to the selected signal processing functions to be performed. Likewise, O'Brien does not mentions real time reconfiguration or disclose a device capable of being reconfigured in real time in which the reconfigurable circuit means is reconfigured at a rate that ensures that data input from at least one of a plurality of input channels and output from at least one of a plurality of output channels is processed in accordance with the required sampling rate or sampled data rate in a way that does not cause any signal aliasing and minimizes noise artifacts on any of the operative input and output channels in relation to the selected signal processing functions to be performed.

Further, the final rejection asserts that the claim limitation of a host processor and associated program memory

means for updating configuration data in the local memory and controlling and monitoring operation of the apparatus is taught by O'Brien's disclosure of a host processor, and an assertion that "it is inherent that DSP and ASIC will contain amounts of memory." Applicant respectfully disagrees. Applicant's claimed host processor and associated program memory means performs a specified function, i.e., "updating configuration data in the local memory and controlling and monitoring operation of the apparatus." While DSP's and ASIC's may contain memory, they do not inherently, i.e., always and necessarily, perform the claimed function. Nor is that function taught by O'Brien. Accordingly, this claimed element is not taught or disclosed in the cited patent.

For at least these reasons, Applicants respectfully submit that claim 1, as well as all the claims dependent therefrom, now distinguishes patentably over the applied reference.

All of the other prior art rejections are traversed for the reason that the rejected claims depend from claim 1, and should be considered allowable along therewith.

If the above amendment should not now place the application in condition for allowance, the Examiner is

invited to call undersigned counsel to resolve any remaining issues.

Respectfully submitted,

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